503 Penny **60

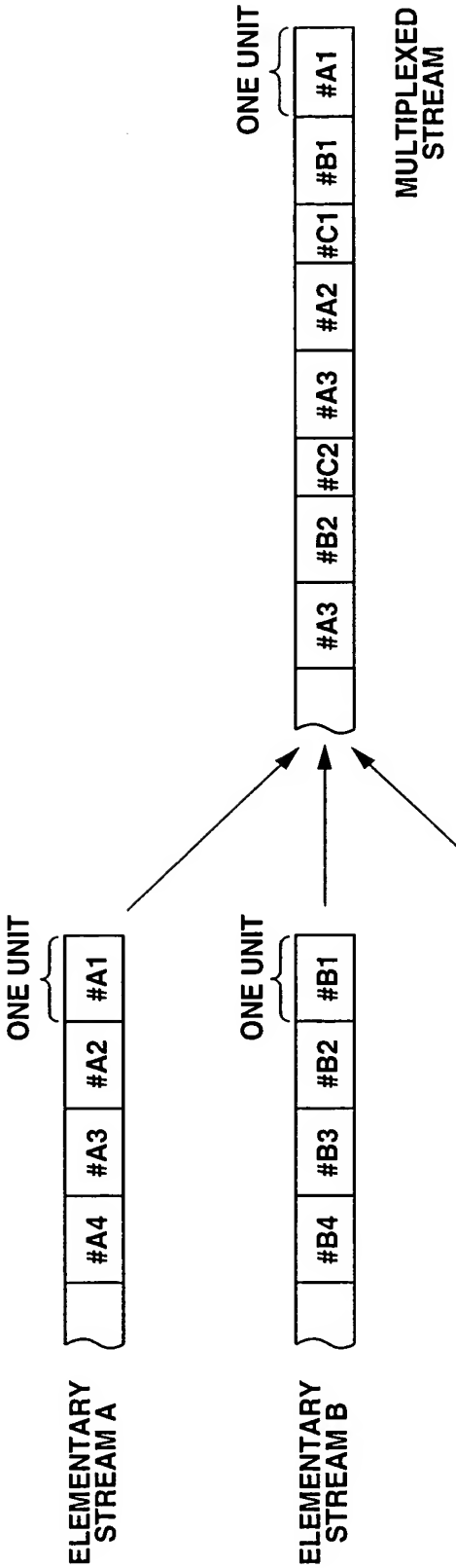

FIG.1

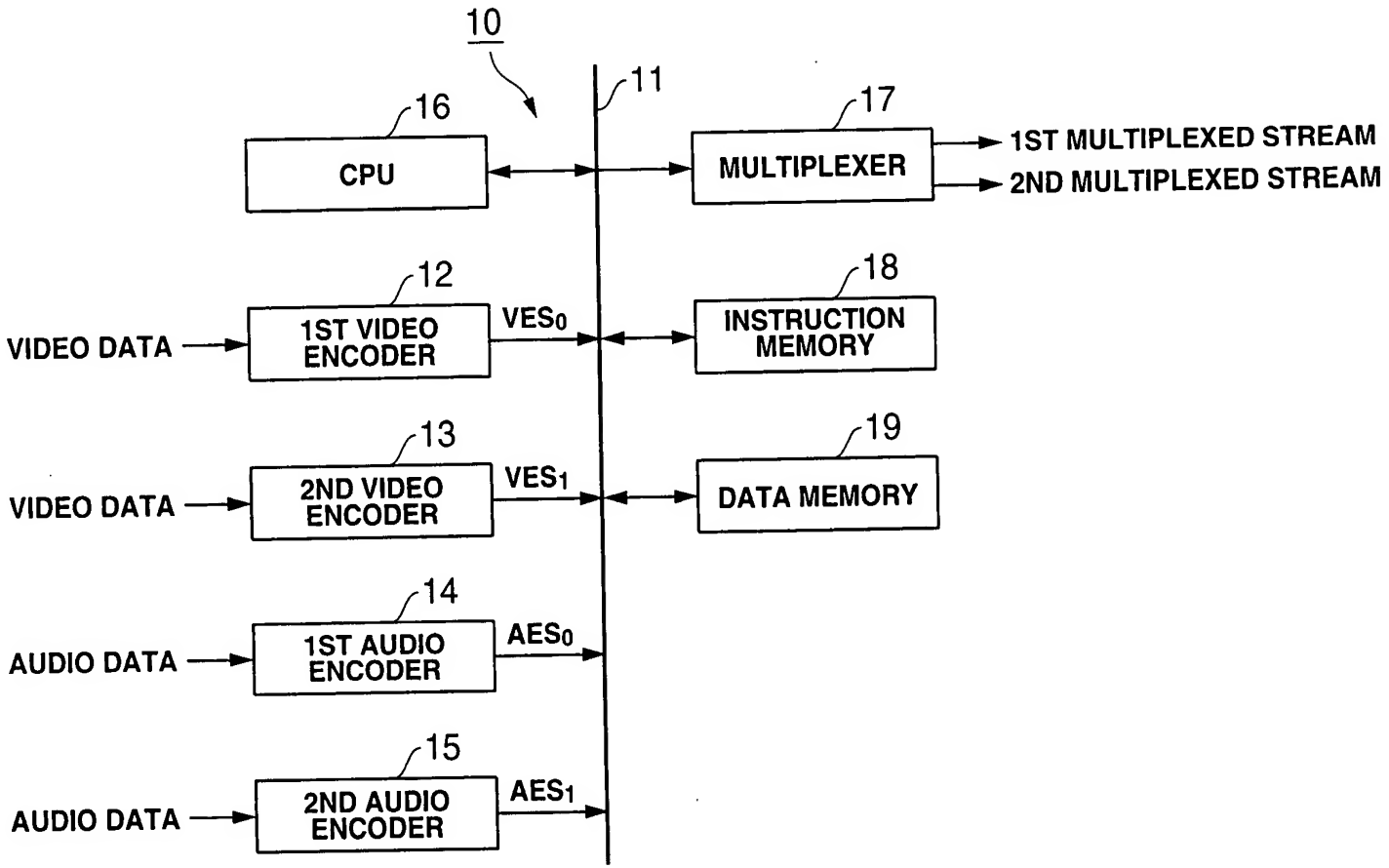
10
11
16
CPU
17
MULTIPLEXER
1ST MULTIPLEXED STREAM
2ND MULTIPLEXED STREAM
12
1ST VIDEO ENCODER
VES0
VIDEO DATA
18
INSTRUCTION MEMORY
13
2ND VIDEO ENCODER
VES1
VIDEO DATA
19
DATA MEMORY
14
1ST AUDIO ENCODER
AES0
AUDIO DATA
15
2ND AUDIO ENCODER
AES1
AUDIO DATA

FIG.2

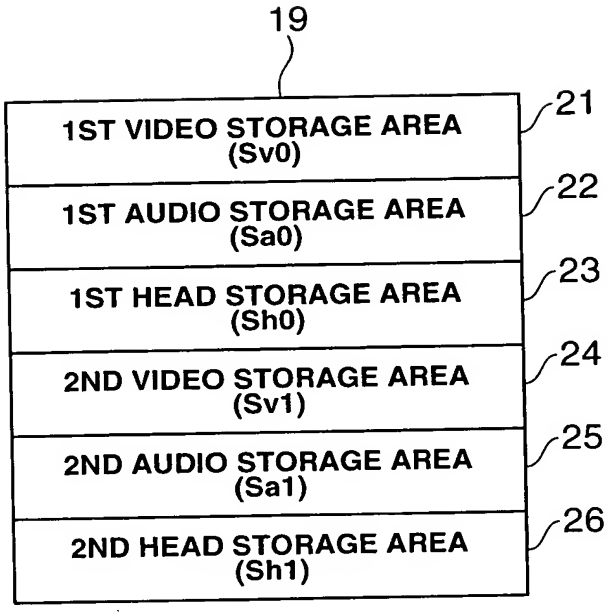
19
1ST VIDEO STORAGE AREA (Sv0)
21
1ST AUDIO STORAGE AREA (Sa0)
22
1ST HEAD STORAGE AREA (Sh0)
23
2ND VIDEO STORAGE AREA (Sv1)
24
2ND AUDIO STORAGE AREA (Sa1)
25
2ND HEAD STORAGE AREA (Sh1)
26

FIG.3

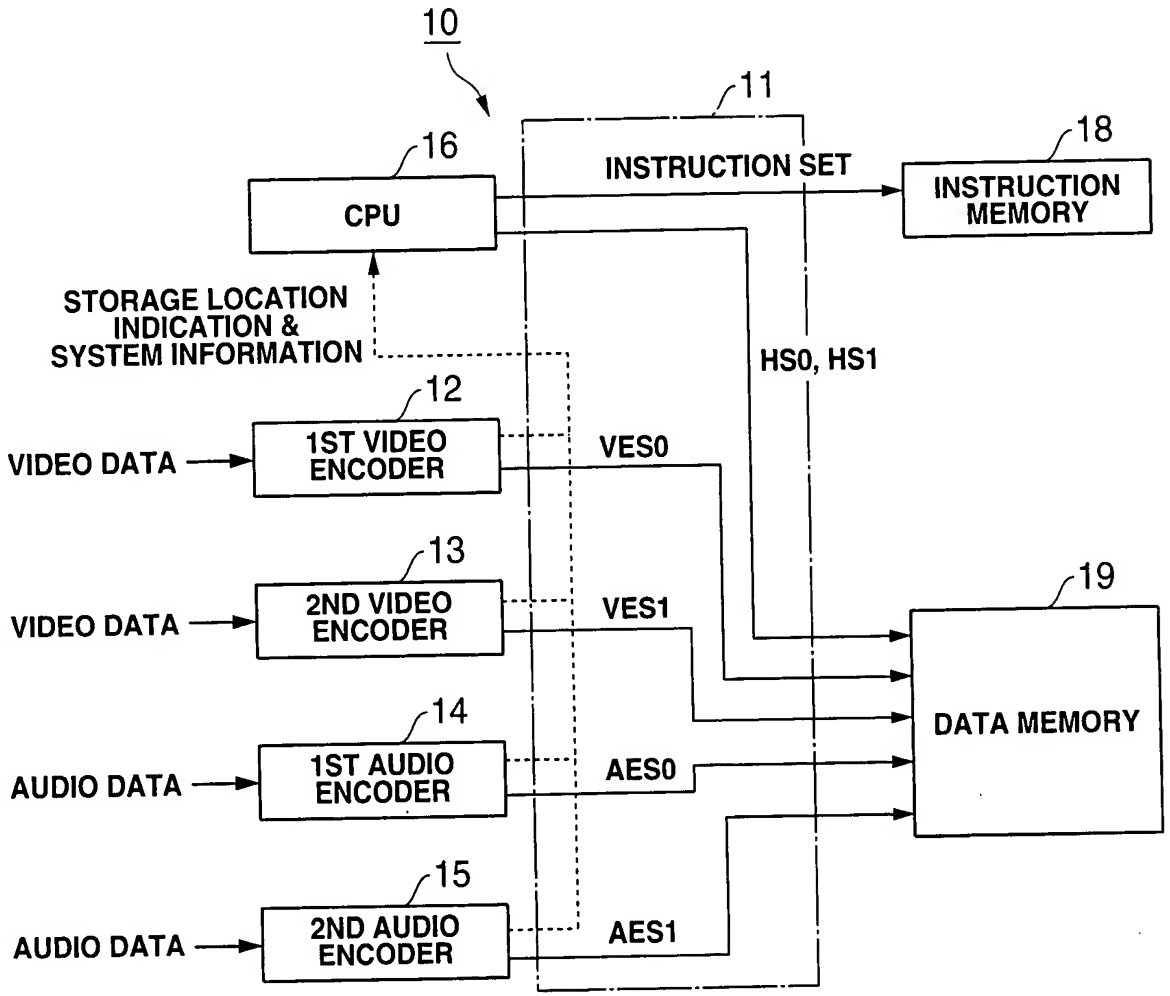
10
11
16
CPU
INSTRUCTION SET
18
INSTRUCTION MEMORY
STORAGE LOCATION INDICATION & SYSTEM INFORMATION
HS0, HS1
12
VIDEO DATA
1ST VIDEO ENCODER
VES0
13
VIDEO DATA
2ND VIDEO ENCODER
VES1
19
DATA MEMORY
14
AUDIO DATA
1ST AUDIO ENCODER
AES0
15
AUDIO DATA
2ND AUDIO ENCODER
AES1

FIG.4

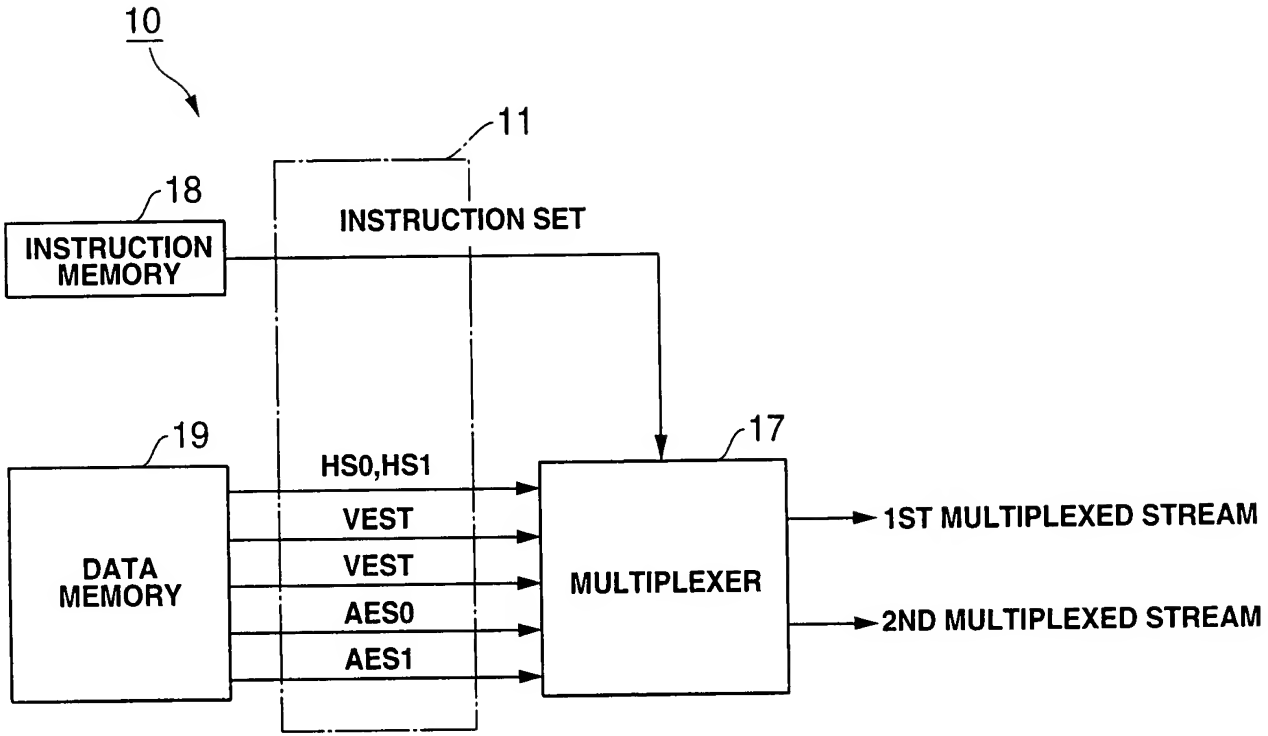
10
11
18
INSTRUCTION MEMORY
INSTRUCTION SET
19
DATA MEMORY
HS0,HS1
VEST
VEST
AES0
AES1
17
MULTIPLEXER
1ST MULTIPLEXED STREAM
2ND MULTIPLEXED STREAM

FIG.5

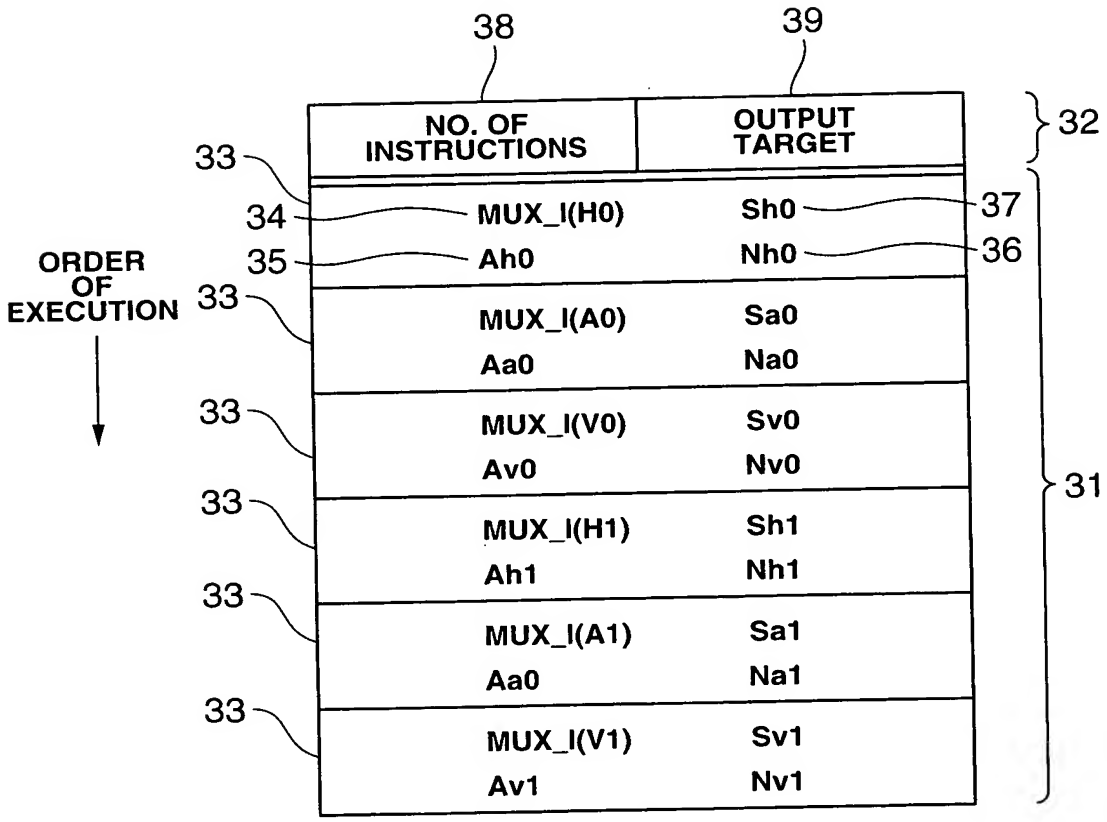
38
39
NO. OF INSTRUCTIONS
OUTPUT TARGET
32
33
34
MUX_I(H0)
Sh0
37
35
Ah0
Nh0
36
ORDER OF EXECUTION
33
MUX_I(A0)
Sa0
Aa0
Na0
33
MUX_I(V0)
Sv0
Av0
Nv0
31
33
MUX_I(H1)
Sh1
Ah1
Nh1
33
MUX_I(A1)
Sa1
Aa0
Na1
33
MUX_I(V1)
Sv1
Av1
Nv1

FIG.6

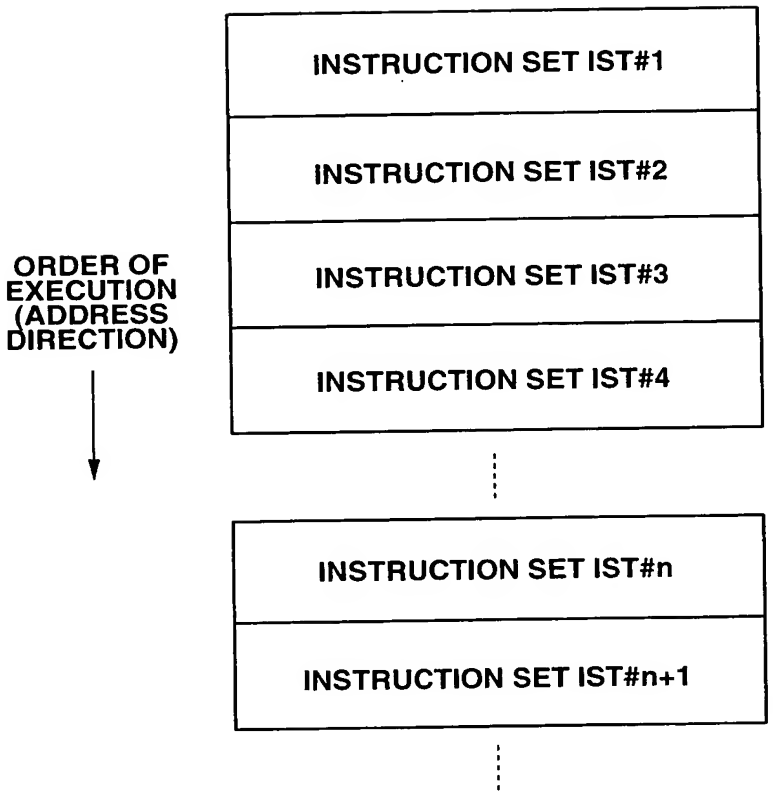
ORDER OF EXECUTION (ADDRESS DIRECTION)
INSTRUCTION SET IST#1
INSTRUCTION SET IST#2
INSTRUCTION SET IST#3
INSTRUCTION SET IST#4
INSTRUCTION SET IST#n
INSTRUCTION SET IST#n+1

FIG.7

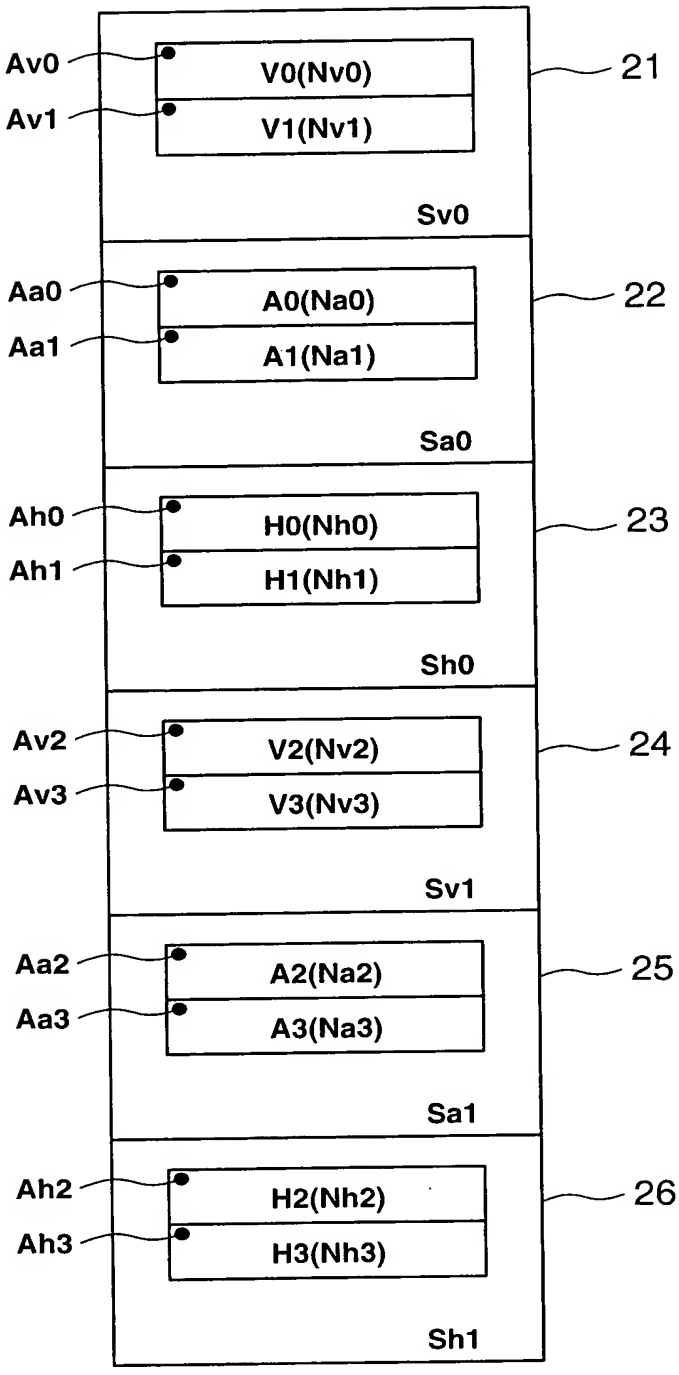
Av0
Av1
V0(Nv0)
V1(Nv1)
21
Sv0
Aa0
Aa1
A0(Na0)
A1(Na1)
22
Sa0
Ah0
Ah1
H0(Nh0)
H1(Nh1)
23
Sh0
Av2
Av3
V2(Nv2)
V3(Nv3)
24
Sv1
Aa2
Aa3
A2(Na2)
A3(Na3)
25
Sa1
Ah2
Ah3
H2(Nh2)
H3(Nh3)
26
Sh1

FIG.8

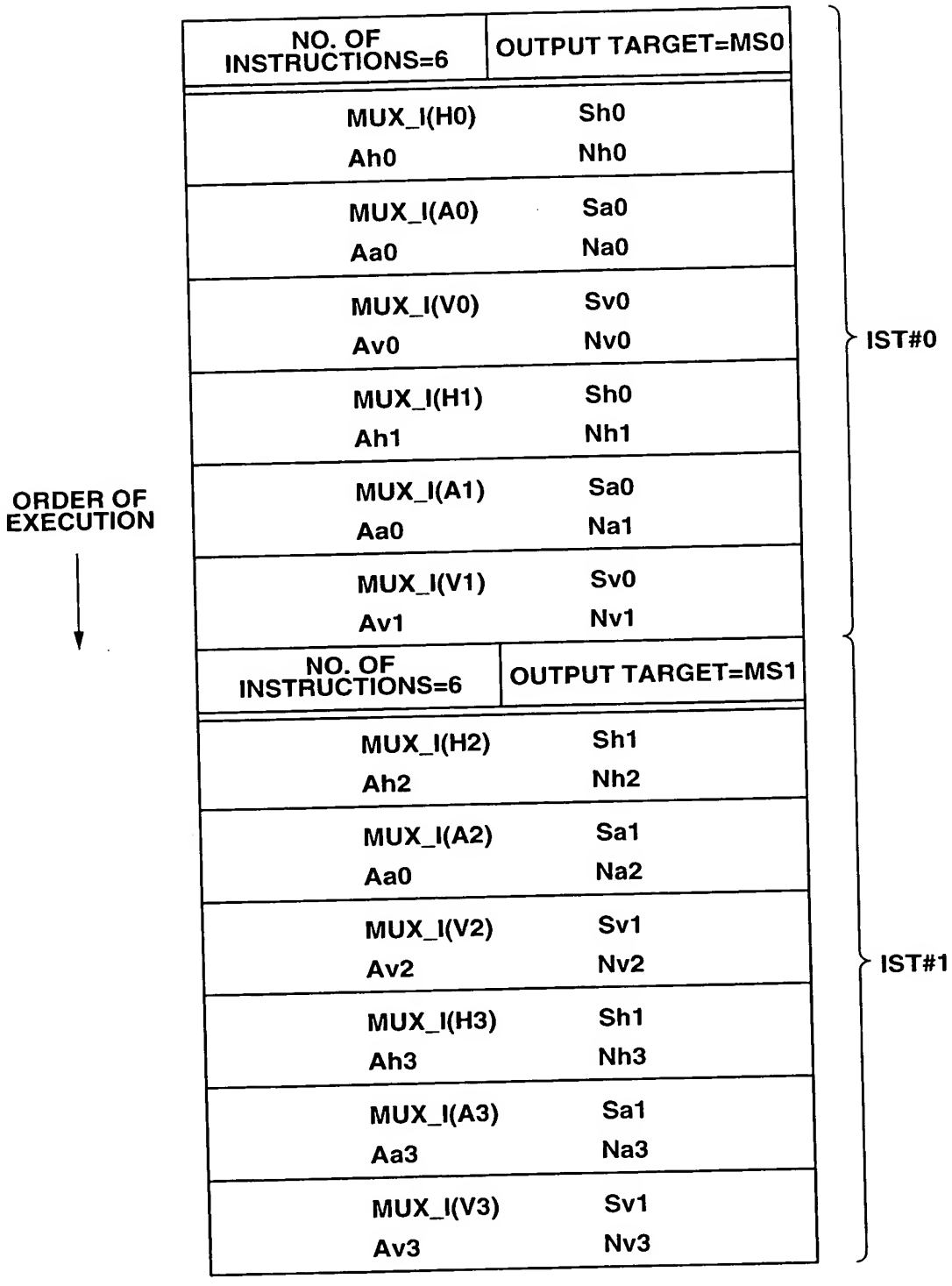
NO. OF INSTRUCTIONS=6
OUTPUT TARGET=MS0
MUX_I(H0) Sh0
Ah0 Nh0
MUX_I(A0) Sa0
Aa0 Na0
MUX_I(V0) Sv0
Av0 Nv0
MUX_I(H1) Sh0
Ah1 Nh1
MUX_I(A1) Sa0
Aa0 Na1
MUX_I(V1) Sv0
Av1 Nv1
IST#0
ORDER OF EXECUTION
NO. OF INSTRUCTIONS=6
OUTPUT TARGET=MS1
MUX_I(H2) Sh1
Ah2 Nh2
MUX_I(A2) Sa1
Aa0 Na2
MUX_I(V2) Sv1
Av2 Nv2
MUX_I(H3) Sh1
Ah3 Nh3
MUX_I(A3) Sa1
Aa3 Na3
MUX_I(V3) Sv1
Av3 Nv3
IST#1

FIG.9

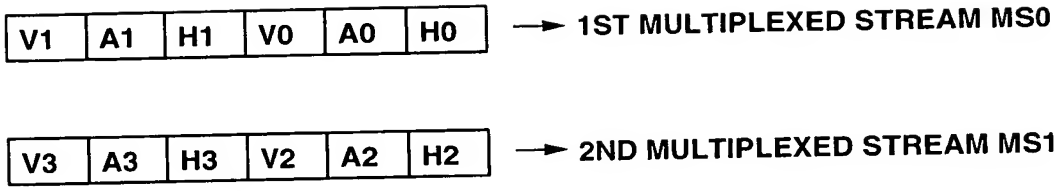
V1
A1
H1
V0
A0
H0
1ST MULTIPLEXED STREAM MS0
V3
A3
H3
V2
A2
H2
2ND MULTIPLEXED STREAM MS1

FIG.10

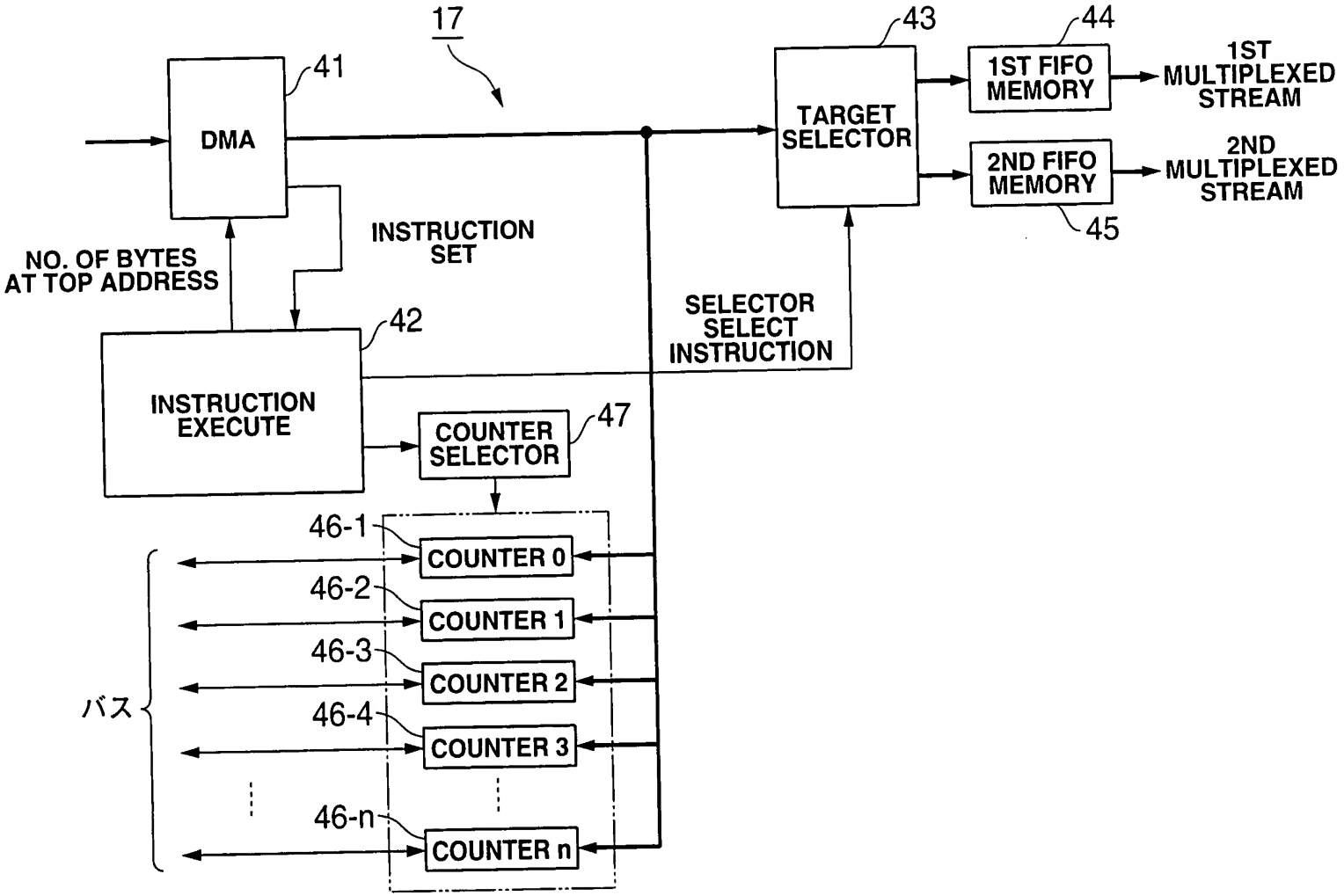
17
41
DMA
43
44
TARGET SELECTOR
1ST FIFO MEMORY
1ST MULTIPLEXED STREAM
2ND FIFO MEMORY
2ND MULTIPLEXED STREAM
45
INSTRUCTION SET
NO. OF BYTES AT TOP ADDRESS
SELECTOR SELECT INSTRUCTION
42
INSTRUCTION EXECUTE
COUNTER SELECTOR
47
46-1
COUNTER 0
46-2
COUNTER 1
46-3
COUNTER 2
46-4
COUNTER 3
46-n
COUNTER n
バス

FIG.11

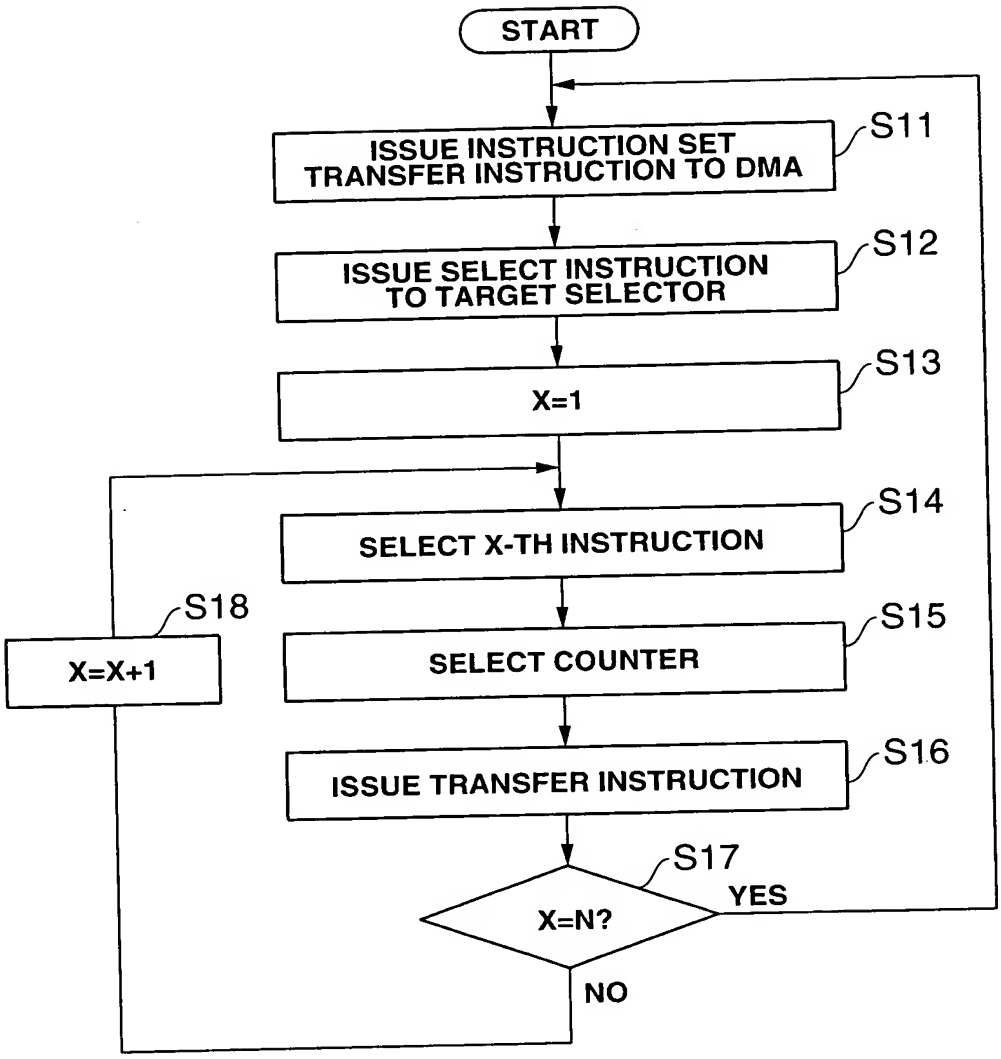
START
ISSUE INSTRUCTION SET TRANSFER INSTRUCTION TO DMA
S11
ISSUE SELECT INSTRUCTION TO TARGET SELECTOR
S12
X=1
S13
SELECT X-TH INSTRUCTION
S14
SELECT COUNTER
S15
ISSUE TRANSFER INSTRUCTION
S16
X=N?
S17
YES
NO
X=X+1
S18

FIG.12

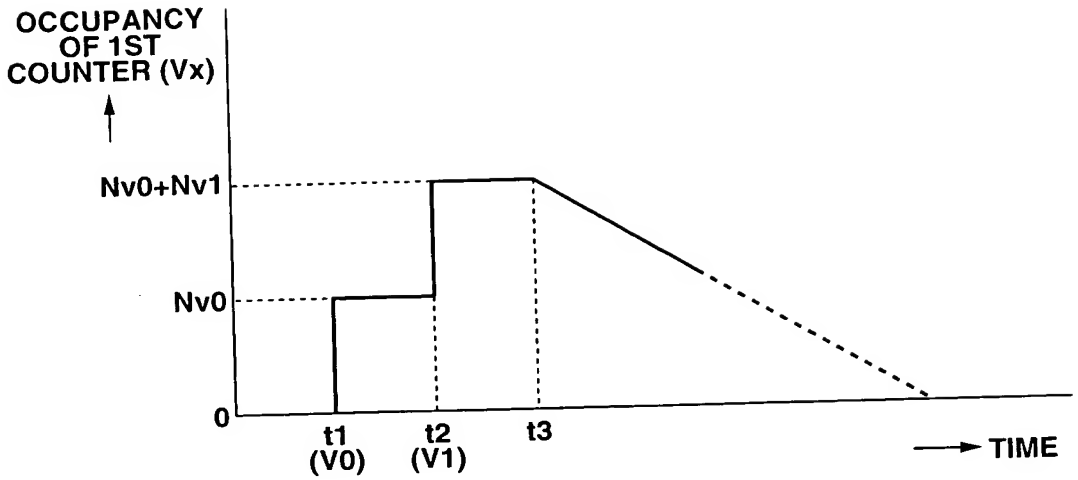
OCCUPANCY
OF 1ST
COUNTER (Vx)
Nv0+Nv1
Nv0
0
t1
(V0)
t2
(V1)
t3
TIME

FIG.13

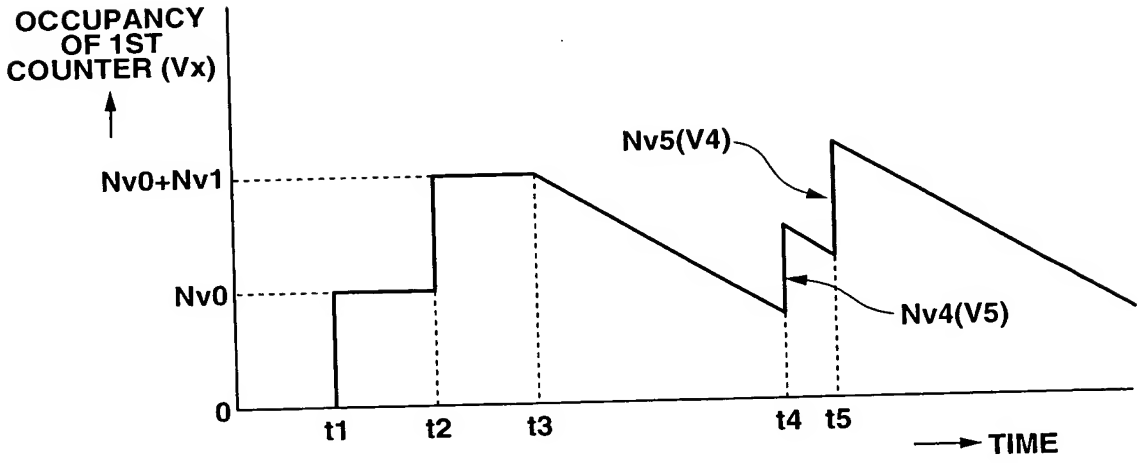
OCCUPANCY
OF 1ST
COUNTER (Vx)
Nv5(V4)
Nv0+Nv1
Nv0
Nv4(V5)
0
t1
t2
t3
t4
t5
TIME

FIG.14

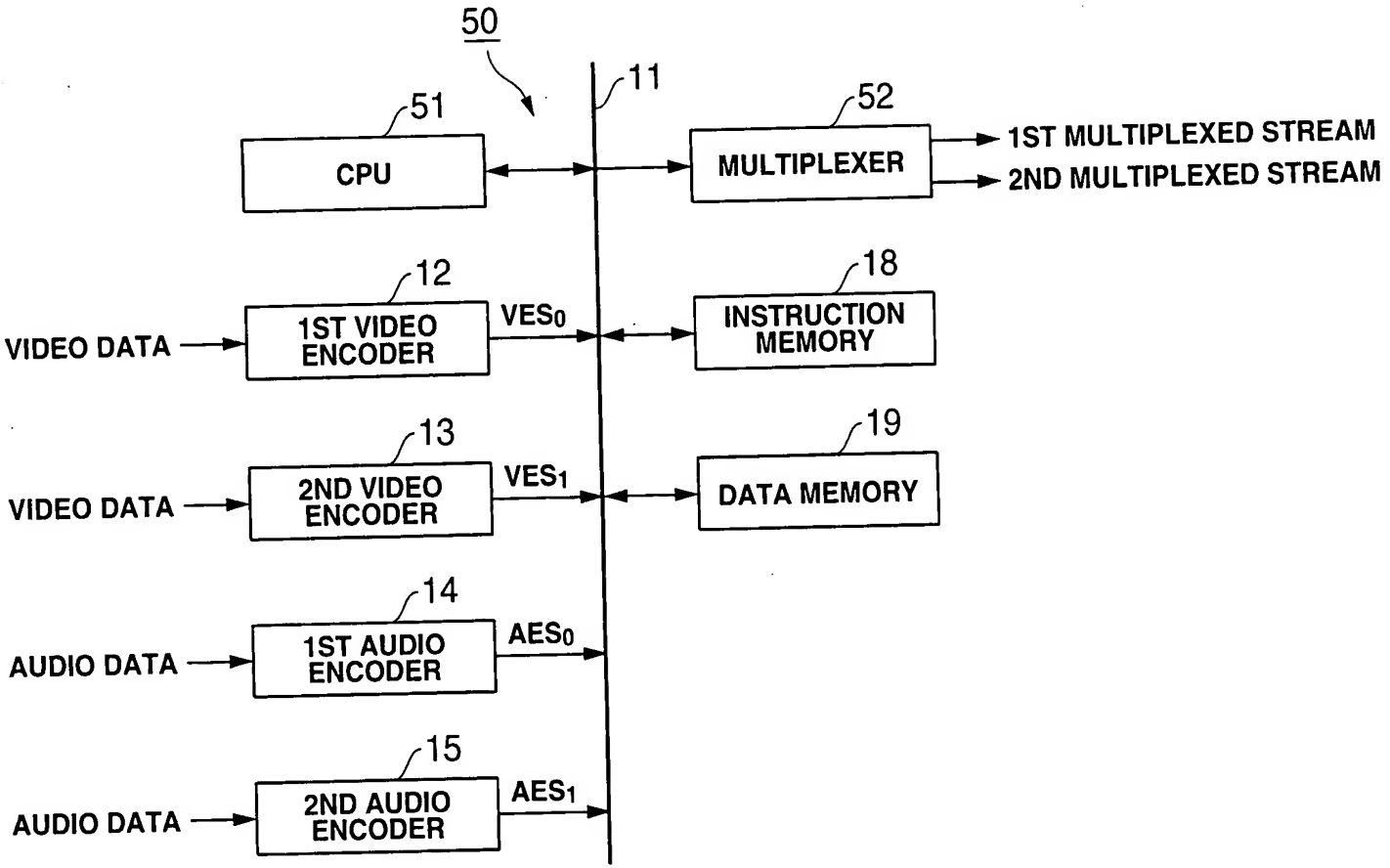
50
11
51
CPU
52
MULTIPLEXER
1ST MULTIPLEXED STREAM
2ND MULTIPLEXED STREAM
12
1ST VIDEO ENCODER
VES0
VIDEO DATA
18
INSTRUCTION MEMORY
13
2ND VIDEO ENCODER
VES1
VIDEO DATA
19
DATA MEMORY
14
1ST AUDIO ENCODER
AES0
AUDIO DATA
15
2ND AUDIO ENCODER
AES1
AUDIO DATA

FIG.15

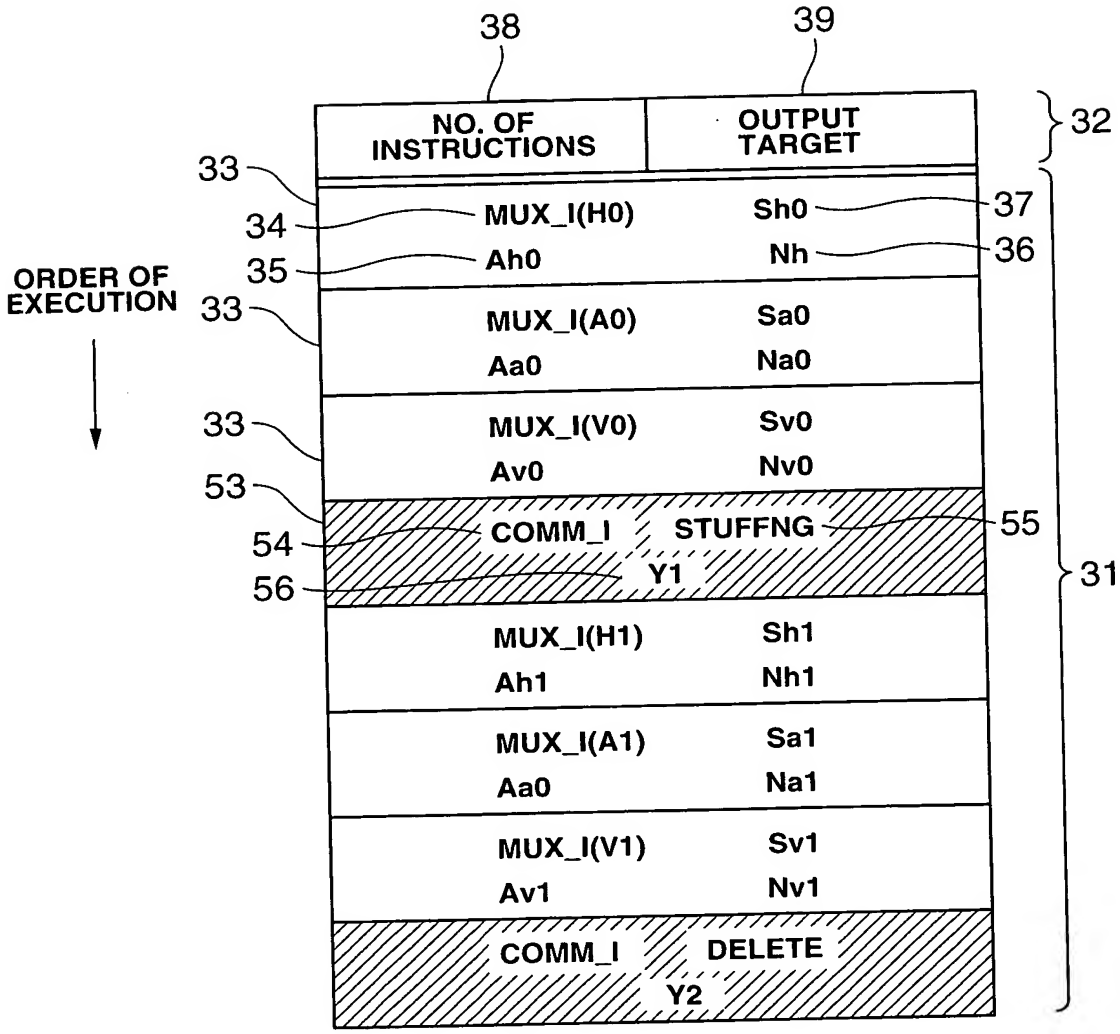
38
39
NO. OF INSTRUCTIONS
OUTPUT TARGET
32
33
34
35
33
33
53
54
56
ORDER OF EXECUTION
MUX_I(H0)
Sh0
37
Ah0
Nh
36
MUX_I(A0)
Sa0
Aa0
Na0
MUX_I(V0)
Sv0
Av0
Nv0
COMM_I
STUFFNG
55
Y1
MUX_I(H1)
Sh1
Ah1
Nh1
MUX_I(A1)
Sa1
Aa0
Na1
MUX_I(V1)
Sv1
Av1
Nv1
COMM_I
DELETE
Y2
31

FIG.16

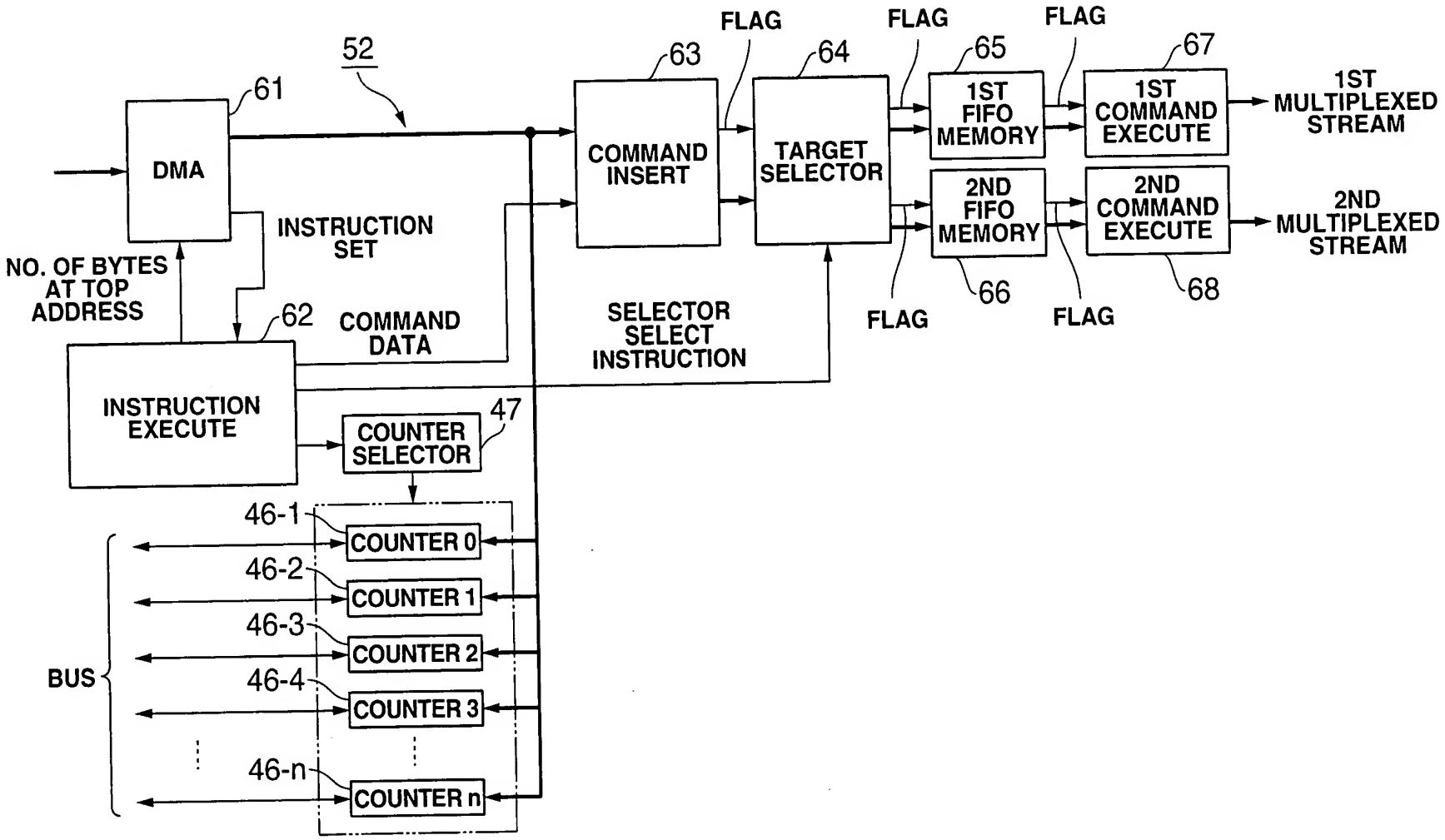
52
61
DMA
INSTRUCTION SET
NO. OF BYTES AT TOP ADDRESS
62
COMMAND DATA
INSTRUCTION EXECUTE
COUNTER SELECTOR
47
46-1
COUNTER 0
46-2
COUNTER 1
46-3
COUNTER 2
46-4
COUNTER 3
46-n
COUNTER n
BUS
63
COMMAND INSERT
FLAG
64
TARGET SELECTOR
SELECTOR SELECT INSTRUCTION
FLAG
65
1ST FIFO MEMORY
2ND FIFO MEMORY
66
FLAG
FLAG
67
1ST COMMAND EXECUTE
2ND COMMAND EXECUTE
68
1ST MULTIPLEXED STREAM
2ND MULTIPLEXED STREAM

FIG.17

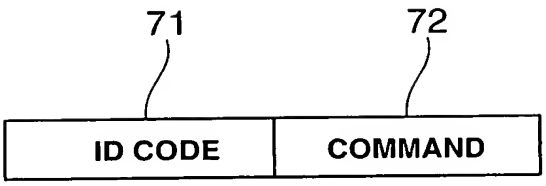

FIG.18

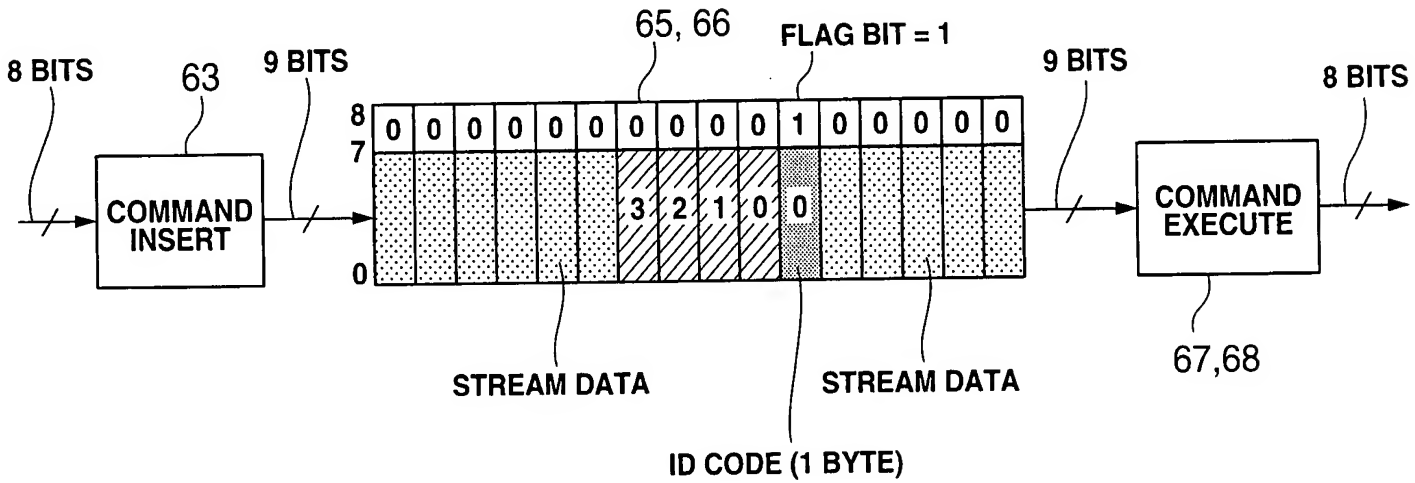
8 BITS
63
9 BITS
65, 66
FLAG BIT = 1
9 BITS
8 BITS
COMMAND INSERT
8
7
0
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
3 2 1 0 0
COMMAND EXECUTE
67,68
STREAM DATA
STREAM DATA
ID CODE (1 BYTE)

FIG.19

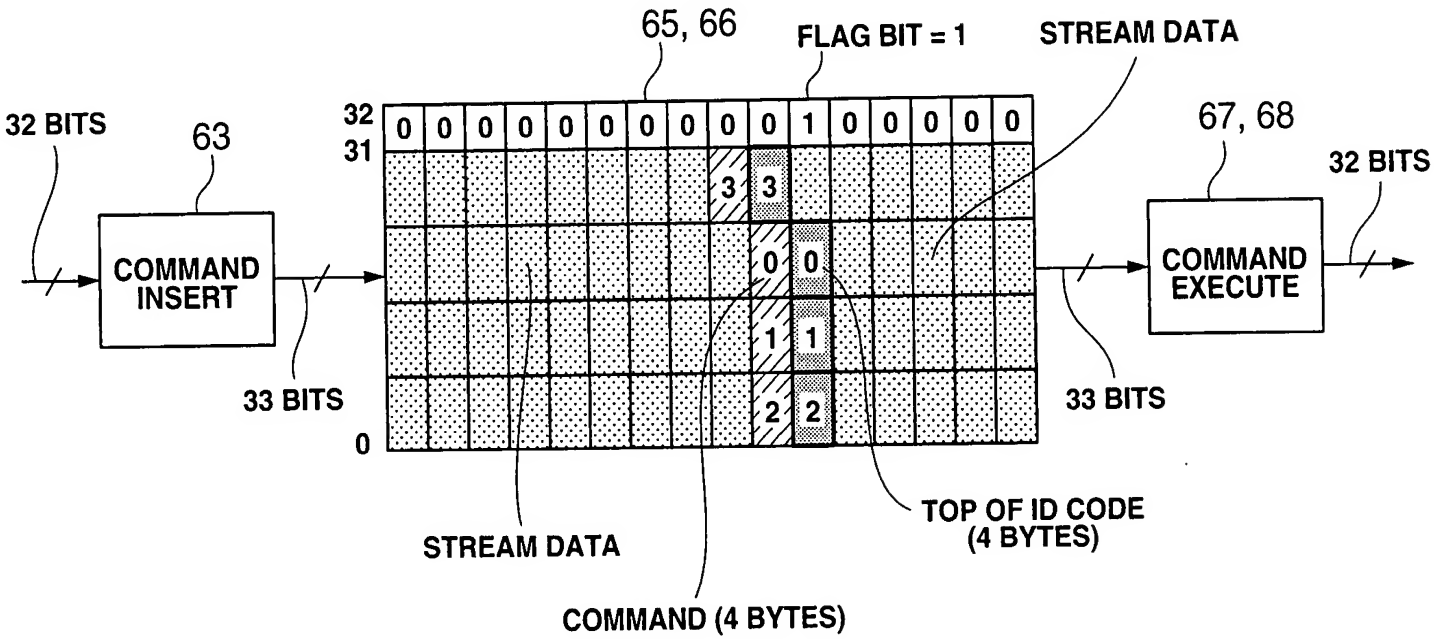
65, 66
FLAG BIT = 1
STREAM DATA
32 BITS
63
32
31
0
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
3 3
0 0
1 1
2 2
67, 68
32 BITS
COMMAND INSERT
COMMAND EXECUTE
33 BITS
33 BITS
STREAM DATA
COMMAND (4 BYTES)
TOP OF ID CODE (4 BYTES)

FIG.20

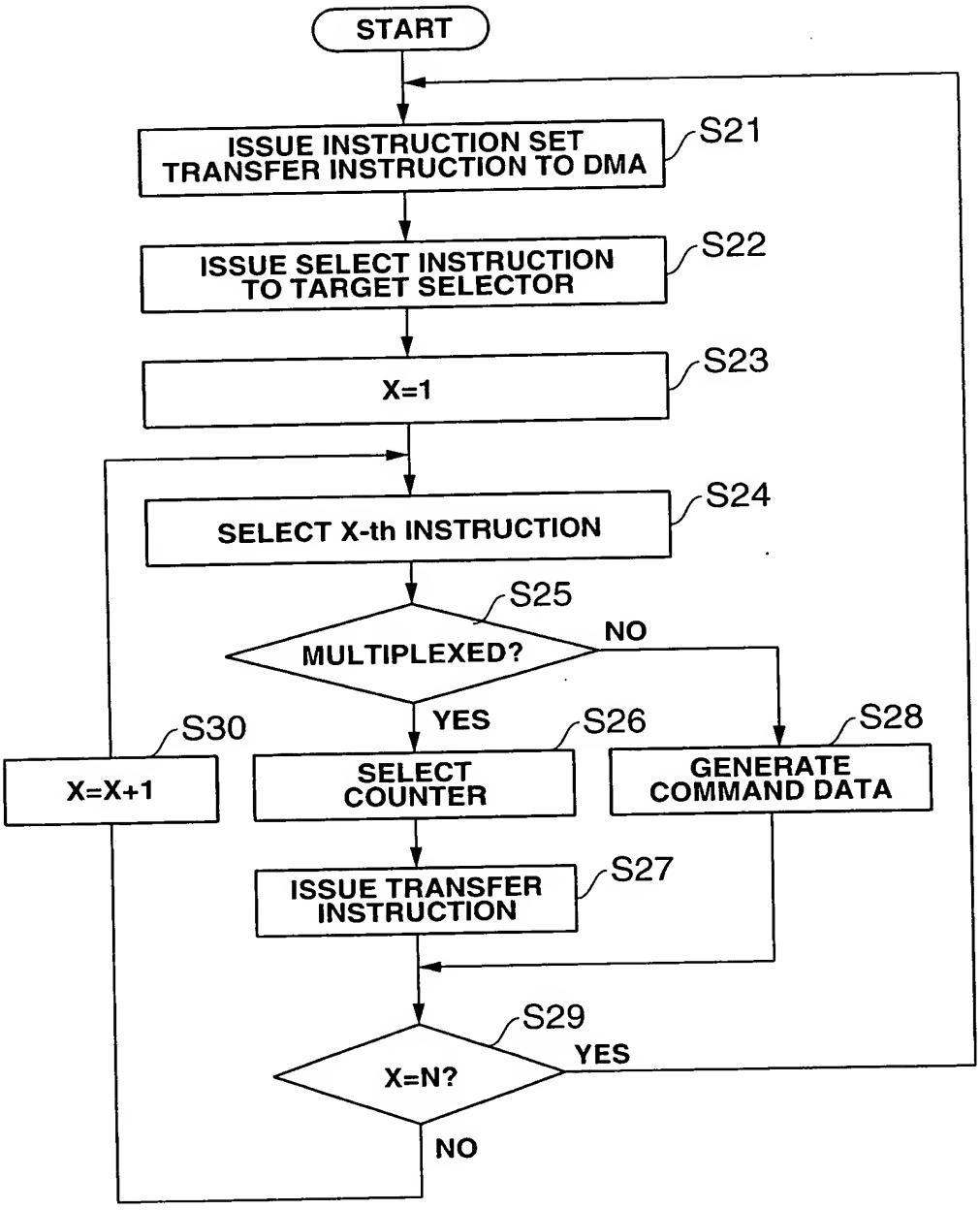
START
ISSUE INSTRUCTION SET TRANSFER INSTRUCTION TO DMA
S21
ISSUE SELECT INSTRUCTION TO TARGET SELECTOR
S22
X=1
S23
SELECT X-th INSTRUCTION
S24
MULTIPLEXED?
S25
NO
YES
X=X+1
S30
SELECT COUNTER
S26
GENERATE COMMAND DATA
S28
ISSUE TRANSFER INSTRUCTION
S27
X=N?
S29
YES
NO

FIG.21

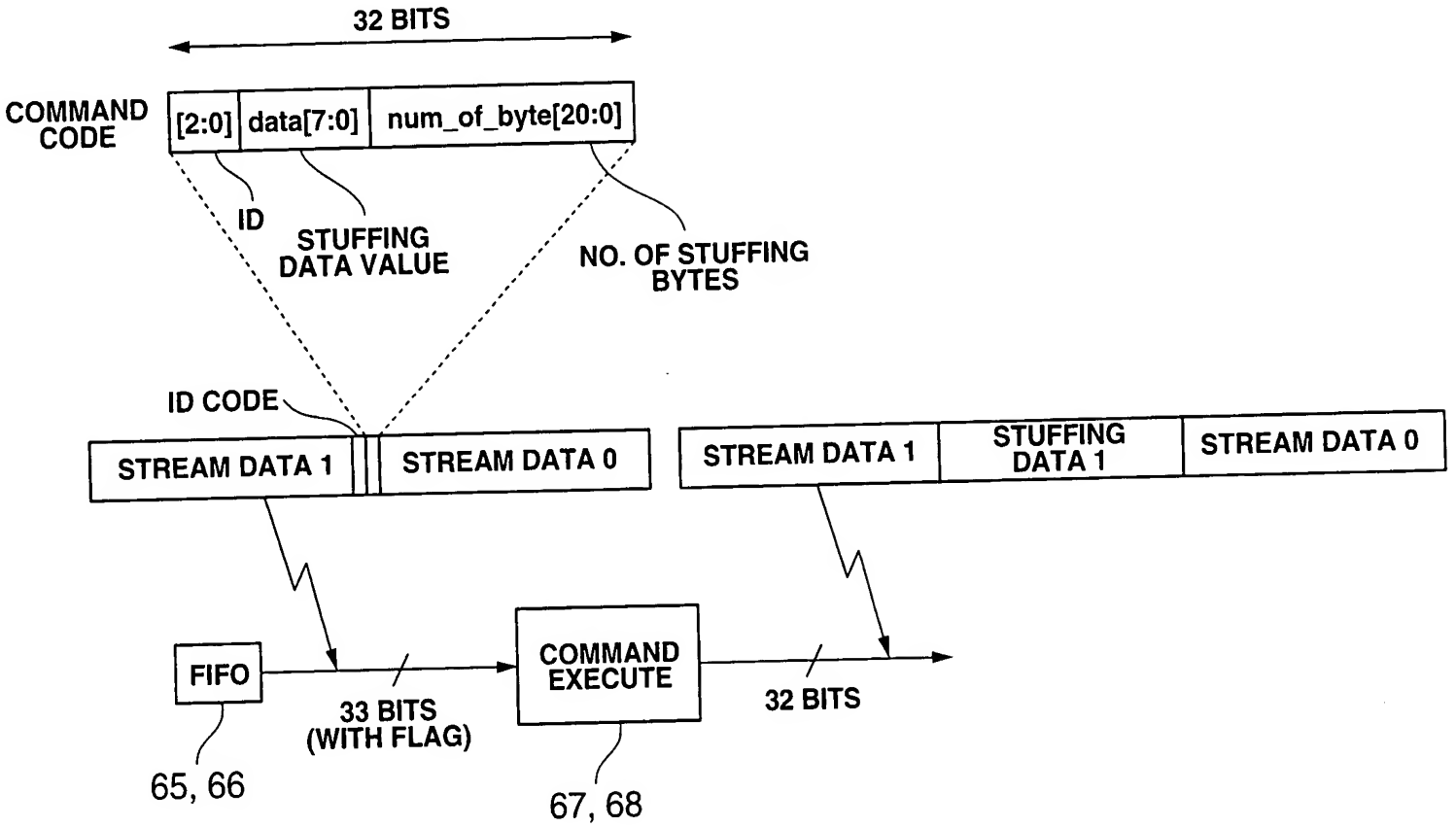
32 BITS
COMMAND CODE
[2:0]
data[7:0]
num_of_byte[20:0]
ID
STUFFING DATA VALUE
NO. OF STUFFING BYTES
ID CODE
STREAM DATA 1
STREAM DATA 0
STREAM DATA 1
STUFFING DATA 1
STREAM DATA 0
FIFO
33 BITS (WITH FLAG)
COMMAND EXECUTE
32 BITS
65, 66
67, 68

FIG.22

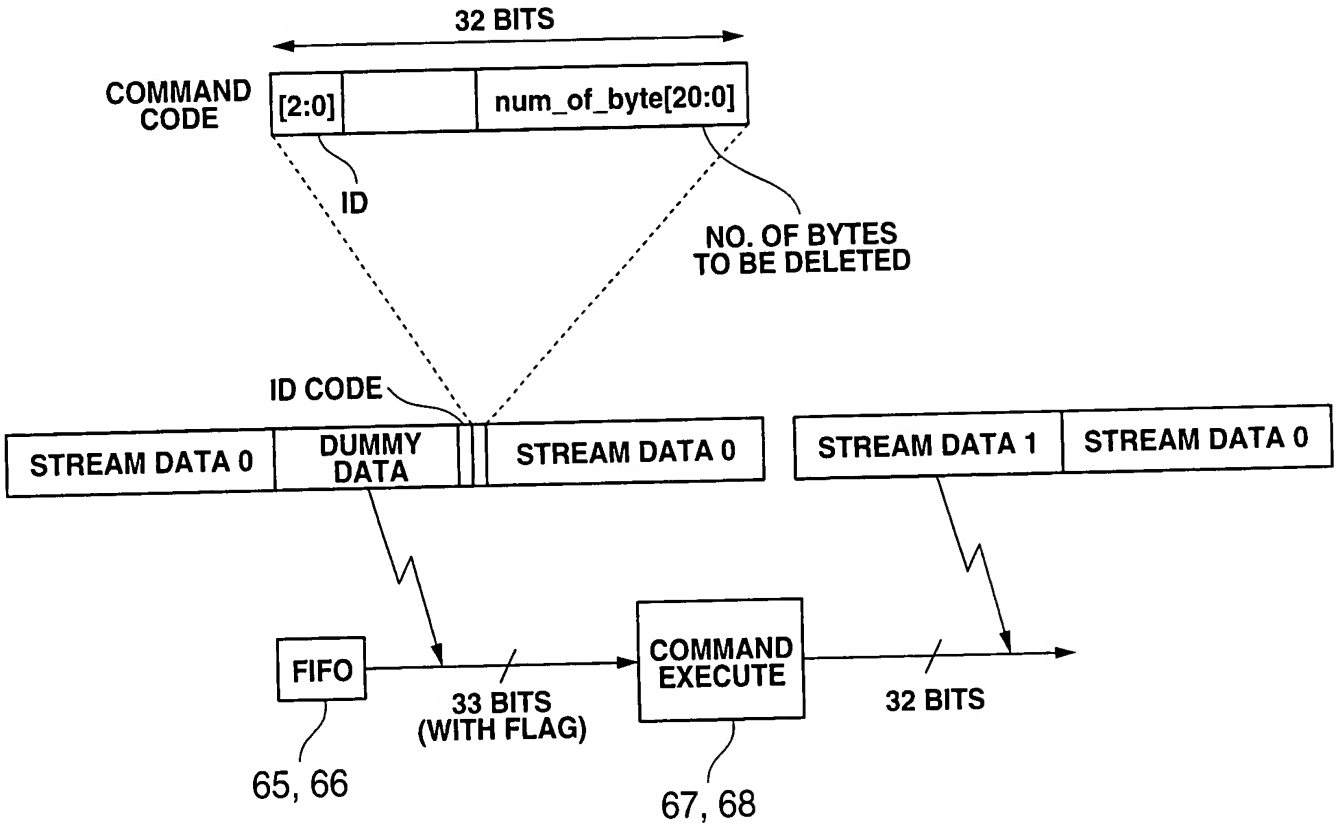
32 BITS
COMMAND CODE
[2:0]
num_of_byte[20:0]
ID
NO. OF BYTES TO BE DELETED
ID CODE
STREAM DATA 0
DUMMY DATA
STREAM DATA 0
STREAM DATA 1
STREAM DATA 0
FIFO
33 BITS (WITH FLAG)
COMMAND EXECUTE
32 BITS
65, 66
67, 68

FIG.23

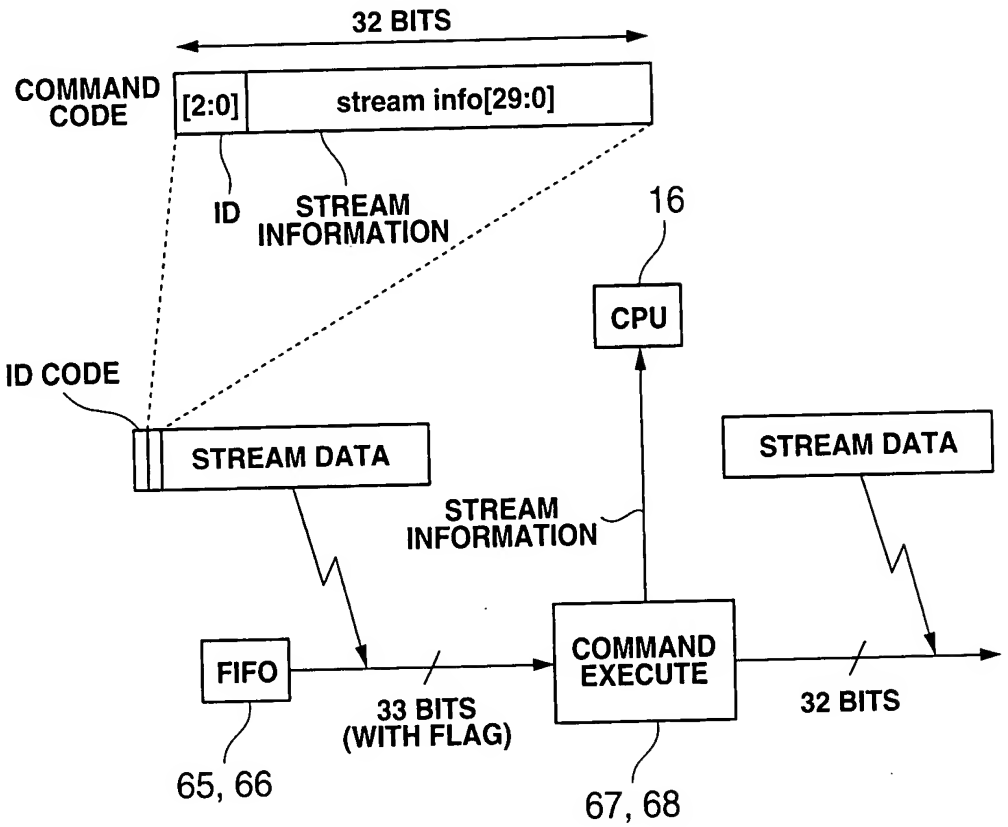
32 BITS
COMMAND CODE
[2:0]
stream info[29:0]
ID
STREAM INFORMATION
16
CPU
ID CODE
STREAM DATA
STREAM DATA
STREAM INFORMATION
FIFO
COMMAND EXECUTE
33 BITS (WITH FLAG)
32 BITS
65, 66
67, 68

FIG.24

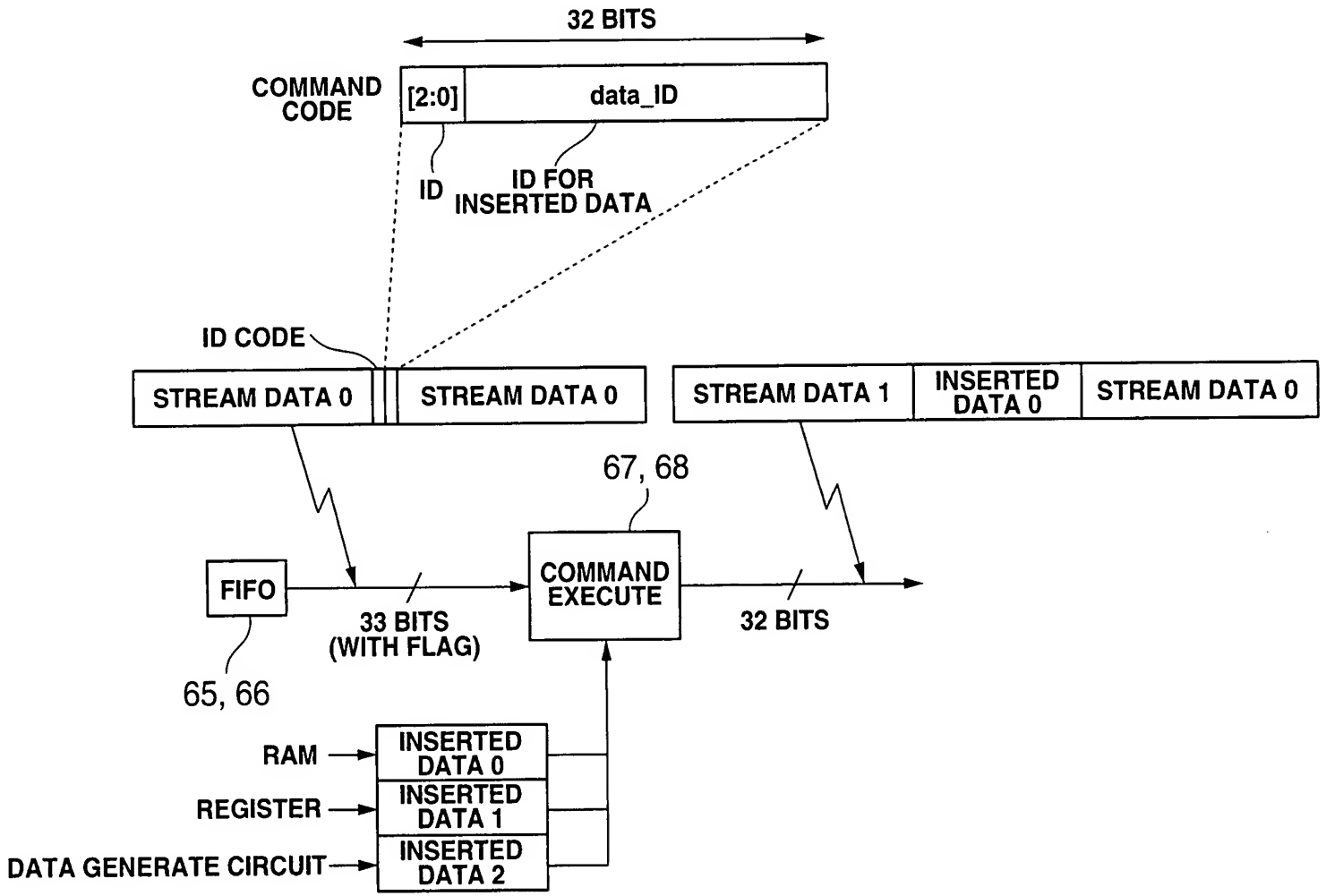
32 BITS
COMMAND CODE
[2:0]
data_ID
ID
ID FOR INSERTED DATA
ID CODE
STREAM DATA 0
STREAM DATA 0
STREAM DATA 1
INSERTED DATA 0
STREAM DATA 0
67, 68
FIFO
33 BITS (WITH FLAG)
COMMAND EXECUTE
32 BITS
65, 66
RAM
REGISTER
DATA GENERATE CIRCUIT
INSERTED DATA 0
INSERTED DATA 1
INSERTED DATA 2

FIG.25